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<input type="checkbox"/>	L27	pipeline with (interrupt\$4 or exception\$1)	2341
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<input type="checkbox"/>	L24	flush\$3 with (interrupt\$4 or exception\$1)	2307
<input type="checkbox"/>	L23	L19 OR L22	15
<input type="checkbox"/>	L22	(5740417 OR 5805879 OR 5884061 OR 5949996 OR 5951678 OR 6125443 OR 6192466).PN.	7
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<input type="checkbox"/>	L14	(part with flush\$3) same pipeline\$1 same (interrupt\$4 or exception\$1)	8
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<input type="checkbox"/>	L13	(part with flush\$3) and pipeline\$1 and (interrupt\$4 or exception\$1)	0
<input type="checkbox"/>	L12	L11 not L10	0
<input type="checkbox"/>	L11	(partial\$2 with flush\$3) and pipeline\$1 and (interrupt\$4 or exception\$1)	2
<input type="checkbox"/>	L10	partial\$2 with flush\$3 with pipeline\$1	5
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<input type="checkbox"/>	L8	L7 not L5	24
<input type="checkbox"/>	L7	L6 with (interrupt\$4 or exception\$1)	28
<input type="checkbox"/>	L6	partial\$2 with flush\$3	4494
<input type="checkbox"/>	L5	L3 same (interrupt\$4 or exception\$1)	9
<input type="checkbox"/>	L4	L3 with (interrupt\$4 or exception\$1)	2
<input type="checkbox"/>	L3	partial\$2 with flush\$3 with pipeline\$1	33

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Laurent Amsaleg, Michael J. Franklin, Olivier Gruber

 August 1999 **ACM Transactions on Computer Systems (TOCS)**, Volume 17 Issue 3

Publisher: ACM Press

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We describe an efficient server-based algorithm for garbage collecting persistent object stores in a client-server environment. The algorithm is incremental and runs concurrently with client transactions. Unlike previous algorithms, it does not hold any transactional locks on data and does not require callbacks to clients. It is fault-tolerant, but performs very little logging. The algorithm has been designed to be integrated into existing systems, and therefore it works with standard i ...

Keywords: client-server system, logging, persistent object-store, recovery

2 [TIDBITS: speedup via time-delay bit-slicing in ALU design for VLSI technology](#)



Peter Y. T. Hsu, Joseph T. Rahmeh, Edward S. Davidson, Jacob A. Abraham

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D. R. Cheriton, A. Gupta, P. D. Boyle, H. A. Goosen

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Publisher: IEEE Computer Society Press, ACM Press

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VMP is an experimental multiprocessor being developed at Stanford University, suitable for high-performance workstations and server machines. Its primary novelty lies in the use of software management of the per-processor caches and the design decisions in the cache and bus that make this approach feasible. The design and some uniprocessor trace-driven simulations indicating its performance have been reported previously. In this paper, we present our initial experience with the V ...

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1 [The VMP multiprocessor: initial experience, refinements, and performance evaluation](#)



D. R. Cheriton, A. Gupta, P. D. Boyle, H. A. Goosen

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Ricardo Farias, Joseph S. B. Mitchell, Cláudio T. Silva

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3 [Garbage collection for a client-server persistent object store](#)



Laurent Amsaleg, Michael J. Franklin, Olivier Gruber

 August 1999 **ACM Transactions on Computer Systems (TOCS)**, Volume 17 Issue 3


Publisher: ACM Press

 Full text available: [pdf\(267.18 KB\)](#)

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Keywords: client-server system, logging, persistent object-store, recovery

- 4 [Multithreading I: Microarchitectural support for precomputation microthreads](#) 
Robert S. Chappell, Francis Tseng, Adi Yoaz, Yale N. Patt
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society Press


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Research has shown that precomputation microthreads can be useful for improving branch prediction and prefetching. However, it is not obvious how to provide the necessary microarchitectural support, and few details have been given in the literature. By judiciously constraining microthreads, we can easily adapt a superscalar machine to support many simultaneous microthreads. The nature of precomputation microthreads also requires efficient usage of resources. Our proposed implementation addresses ...

- 5 [TIDBITS: speedup via time-delay bit-slicing in ALU design for VLSI technology](#) 
 Peter Y. T. Hsu, Joseph T. Rahmeh, Edward S. Davidson, Jacob A. Abraham
June 1985 **ACM SIGARCH Computer Architecture News , Proceedings of the 12th annual international symposium on Computer architecture ISCA '85**, Volume 13 Issue 3

Publisher: IEEE Computer Society Press, ACM Press

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- 6 [Refinement Maps for Efficient Verification of Processor Models](#) 
Panagiotis Manolios, Sudarshan K. Srinivasan
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Publisher: IEEE Computer Society

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While most of the effort in improving verification times for pipeline machine verification has focused on faster decision procedures, we show that the refinement maps used also have a drastic impact on verification times. We introduce a new class of refinement maps for pipelined machine verification, and using the state-of-the-art verification tools UCLID and Siege we show that one can attain several orders of magnitude improvements in verification times over the standard flushing-based refineme ...

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IEE JNL IEE Journal or Magazine

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**1. Design issues and tradeoffs for write buffers**

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IEEE STD. IEEE Standard

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Volume 50, Issue 6, June 2001 Page(s):529 - 548
Digital Object Identifier 10.1109/12.931892[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(6164 KB) IEEE JNL.**2. Microarchitectural support for precomputation microthreads**Chappell, R.S.; Tseng, F.; Yoaz, A.; Patt, Y.N.; Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on
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